

# VHDL Cheat-Sheet

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<b>Concurrent Statements</b>		<b>Sequential Statements</b>
<b>Concurrent Signal Assignment</b> (dataflow model)	↔	<b>Signal Assignment</b>
<code>target &lt;= expression;</code>		<code>target &lt;= expression;</code>
<code>A &lt;= B AND C; DAT &lt;= (D AND E) OR (F AND G);</code>		<code>A &lt;= B AND C; DAT &lt;= (D AND E) OR (F AND G);</code>
<b>Conditional Signal Assignment</b> (dataflow model)	↔	<b>if statements</b>
<code>target &lt;= expressn when condition else     expressn when condition else     expressn;</code>		<code>if (condition) then     { sequence of statements } elsif (condition) then     { sequence of statements } else --(the else is optional)     { sequence of statements } end if;</code>
<code>F3 &lt;= '1' when (L='0' AND M='0') else     '1' when (L='1' AND M='1') else     '0';</code>		<code>if (SEL = "111") then F_CTRL &lt;= D(7); elsif (SEL = "110") then F_CTRL &lt;= D(6); elsif (SEL = "101") then F_CTRL &lt;= D(1); elsif (SEL = "000") then F_CTRL &lt;= D(0); else F_CTRL &lt;= '0'; end if;</code>
<b>Selective Signal Assignment</b> (dataflow model)	↔	<b>case statements</b>
<code>with chooser_expression select     target &lt;= expression when choices,     expression when choices;</code>		<code>case (expression) is     when choices =&gt;         {sequential statements}     when choices =&gt;         {sequential statements}     when others =&gt; -- (optional)         {sequential statements} end case;</code>
<code>with SEL select MX_OUT &lt;= D3 when "11",           D2 when "10",           D1 when "01",           D0 when "00",           '0' when others;</code>		<code>case ABC is     when "100" =&gt; F_OUT &lt;= '1';     when "011" =&gt; F_OUT &lt;= '1';     when "111" =&gt; F_OUT &lt;= '1';     when others =&gt; F_OUT &lt;= '0'; end case;</code>
<b>Process</b> (behavioral model)		
<code>opt_label: process(sensitivity_list) begin     {sequential_statements} end process opt_label;</code>		
<code>procl: process(A,B,C) begin     if (A = '1' and B = '0') then         F_OUT &lt;= '1';     elsif (B = '1' and C = '1') then         F_OUT &lt;= '1';     else         F_OUT &lt;= '0';     end if; end process procl;</code>		